In the Claims:

The pending claims are presented below.

1. (Original) A circuit arrangement for adding a first binary operand of N bits and a second binary operand of M bits, N being greater than or equal to M, comprising:

an adder adapted to add representative sets of least-significant bits of the first and second binary operands together to produce a least-significant bits partial sum and a carryout; and

a multiplexer circuit coupled to the adder and adapted to output a most-significant bits partial sum by passing one of: a representative set of most-significant bits of the first binary operand, and an offset of the representative set of most-significant bits of the first binary operand, responsive to selection data, the selection data being a function of the most-significant bit of the representative set of least-significant bits of the first binary operand.

2. (Original) The circuit arrangement of claim 1, wherein the adder is an M-bit adder, the representative sets of least-significant bits of the first and second binary operands each have a length of M bits, and the selection data includes a carryout from the M-bit adder, and the Mth bit of the first binary operand.

3. (previously presented) The circuit arrangement of claim 2, wherein the most-significant bits partial sum is one of: N-M most significant bits of the first binary operand, N-M most significant bits of the first binary operand incremented by one, and N-M most significant bits of the first binary operand decremented by one.

4. (Original) The circuit arrangement of claim 3, wherein N is 24 and M is 16.

5. (Original) The circuit arrangement of claim 1, wherein the offset of the representative set of most-significant bits of the first binary operand include a first incremented offset, and a second decremented offset.

6. (Original) The circuit arrangement of claim 5, wherein the first incremented offset is the representative set of most-significant bits of the first binary operand incremented by one, and the second incremented offset is the representative set of most-significant bits of the first binary operand decremented by one.

7. (Original) The circuit arrangement of claim 6, wherein the multiplexer circuit includes a multiplexer adapted to select one of at least three input binary quantities.

8. (Original) The circuit arrangement of claim 1, wherein the selection data includes the most-significant bit of the representative set of least-significant bits of the first binary operand, and a carryout from the adder.

9. (Original) The circuit arrangement of claim 8, wherein the carryout is available from the adder before the least-significant bits partial sum.

10. (Original) The circuit arrangement of claim 1, wherein the offset of the representative set of most-significant bits of the first binary operand include a first incremented offset, and a second decremented offset, wherein the first incremented offset is the representative set of most-significant bits of the first binary operand incremented by one, and the second incremented offset is the representative set of most-significant bits of the first binary operand decremented by one, wherein the selection data includes the most-significant bit of the representative set of least-significant bits of the first binary operand, and a carryout from the adder, and wherein the carryout is available from the adder before the least-significant bits partial sum.

11. (previously presented) The circuit arrangement of claim 1, wherein N-M is one, and the multiplexer circuit is further configured to operate as an exclusive-or gate, the selection data being the most-significant bit of one of the representative sets of the first binary operand and a carryout from the adder.

12. (previously presented) The circuit arrangement of claim 1, wherein N equals M, the most-significant bit of the second binary operand is zero, and the multiplexer circuit is further configured to operate as an exclusive-or gate, the selection data being the most-significant bit of one of the representative sets of the first binary operand and a carryout from the adder.

13. (Original) The circuit arrangement of claim 12, wherein the carryout is available from the adder before the least-significant bits partial sum.

14. (Original) The circuit arrangement of claim 1, wherein the operands are unsigned binary numbers, and the multiplexer circuit is further configured to operate as an exclusive-or gate, the selection data being the most-significant bit of the first binary operand and a carryout from the adder.

15. (Original) The circuit arrangement of claim 1, wherein the operands are unsigned binary numbers.

16. (Original) A digital filtering circuit arrangement, according to claim 1, wherein the adder and the multiplexer are part of a pipelined datapath unit.

17. (Original) The digital filtering circuit arrangement of claim 16, further including a processor and a memory, wherein the processor feeds data through memory to the pipelined datapath unit.

18. (Original) A method for adding a first binary operand of N bits and a second binary operand of M bits, N being greater than or equal to M, comprising:

adding representative sets of least-significant bits of the first and second binary operands together to produce a least-significant bits partial sum and a carryout; and

outputting a most-significant bits partial sum by passing one of: a representative set of most-significant bits of the first binary operand, and an offset of the representative set of most-significant bits of the first binary operand, responsive to selection data, the

selection data being a function of the most-significant bit of the representative set of least-significant bits of the first binary operand.

19. (Original) A circuit arrangement for adding a first binary operand of N bits and a second binary operand of M bits, N being greater than or equal to M, comprising:

means for adding representative sets of least-significant bits of the first and second binary operands together to produce a least-significant bits partial sum and a carryout; and

means for outputting a most-significant bits partial sum by passing one of: a representative set of most-significant bits of the first binary operand, and an offset of the representative set of most-significant bits of the first binary operand, responsive to selection data, the selection data being a function of the most-significant bit of the representative set of least-significant bits of the first binary operand.

20. (previously presented) A circuit arrangement for adding M most-significant bits of a first N-bit binary operand and M most-significant bits of a second N-bit binary operand, comprising:

an adder adapted to add representative sets of least-significant bits of the first and second binary operands together to produce a N-M+1 bit partial sum;

a first multiplexer circuit coupled to the adder and adapted to produce an output representative of the adder's (N-M)th bit internal carry bit, responsive to a first selection data set, the first selection data set including each of the respective (N-M+1)th bits of the binary operands, and the (N-M+1)th bit of the partial sum; and

a second multiplexer circuit coupled to the first multiplexer circuit and adapted to output an most-significant bits partial sum by passing one of: a representative set of most-significant bits of the second binary operand, and an offset of the representative set of most-significant bits of the second binary operand, responsive to the first multiplexer output.